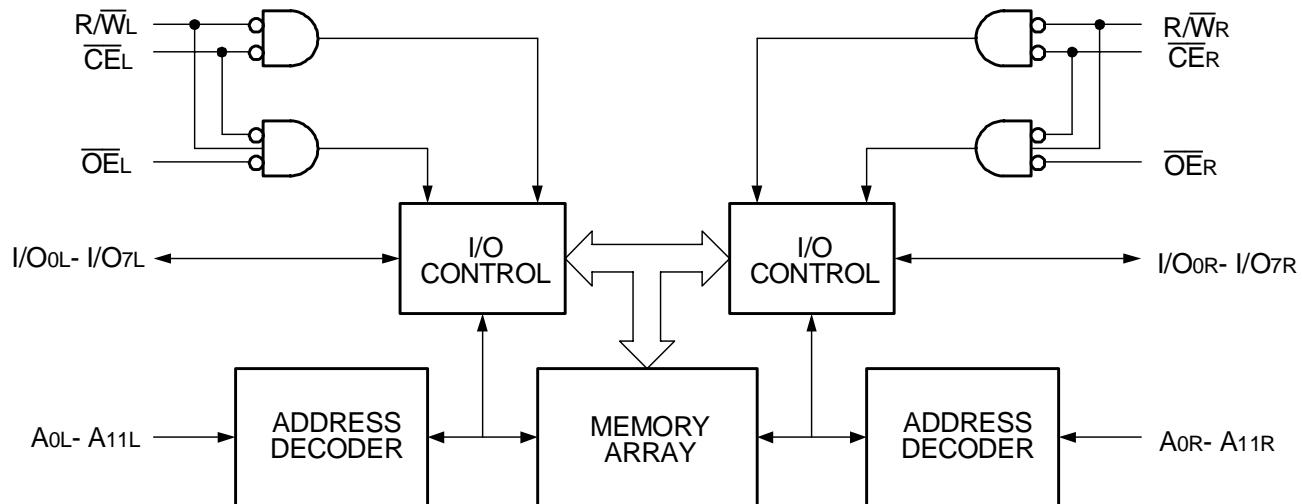


Features

- ◆ **High-speed access**
 - *Military: 25/35/45/55/70ns (max.)*
 - *Industrial: 25/35/55ns (max.)*
 - *Commercial: 20/25/35/45/55/70ns (max.)*
- ◆ **Low-power operation**
 - *IDT7134SA*
Active: 700mW (typ.)
Standby: 5mW (typ.)
 - *IDT7134LA*
Active: 700mW (typ.)
Standby: 1mW (typ.)

- ◆ Fully asynchronous operation from either port
- ◆ Battery backup operation—2V data retention (LA only)
- ◆ TTL-compatible; single 5V ($\pm 10\%$) power supply
- ◆ Available in 48-pin DIP, LCC, Flatpack and 52-pin PLCC
- ◆ Military product compliant to MIL-PRF-38535 QML
- ◆ Industrial temperature range (-40°C to $+85^{\circ}\text{C}$) is available for selected speeds
- ◆ Green parts available, see ordering information

Functional Block Diagram



2720 drw 01

JANUARY 2006

Description

The IDT7134 is a high-speed 4K x 8 Dual-Port Static RAM designed to be used in systems where on-chip hardware port arbitration is not needed. This part lends itself to those systems which cannot tolerate wait states or are designed to be able to externally arbitrate or withstand contention when both sides simultaneously access the same Dual-Port RAM location.

The IDT7134 provides two independent ports with separate control, address, and I/O pins that permit independent, asynchronous access for reads or writes to any location in memory. It is the user's responsibility to ensure data integrity when simultaneously accessing the same memory location from both ports. An automatic power down feature,

controlled by \overline{CE} , permits the on-chip circuitry of each port to enter a very low standby power mode.

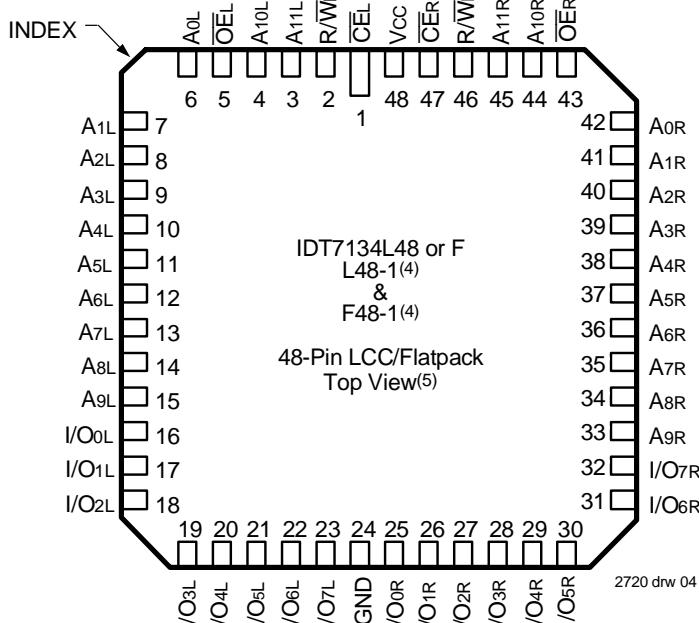
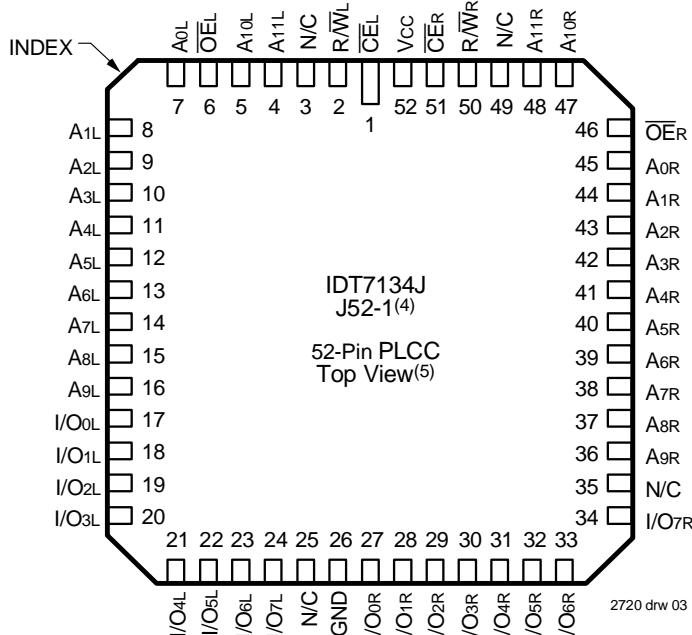
Fabricated using IDT's CMOS high-performance technology, these Dual-Ports typically operate on only 700mW of power. Low-power (LA) versions offer battery backup data retention capability, with each port typically consuming 200 μ W from a 2V battery.

The IDT7134 is packaged on either a sidebrazed or plastic 48-pin DIP, 48-pin LCC, 52-pin PLCC and 48-pin Flatpack. Military grade product is manufactured in compliance with the latest revision of MIL-PRF-38535 QML, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

Pin Configurations^(1,2,3)

\overline{CE}_L	1	48	VCC
$\overline{R/W}_L$	2	47	\overline{CE}_R
A _{11L}	3	46	$\overline{R/W}_R$
A _{10L}	4	45	A _{11R}
\overline{O}_L	5	44	A _{10R}
A _{0L}	6	43	\overline{O}_R
A _{1L}	7	42	A _{0R}
A _{2L}	8	41	A _{1R}
A _{3L}	9	40	A _{2R}
A _{4L}	10	39	A _{3R}
A _{5L}	11	38	A _{4R}
A _{6L}	12	37	A _{5R}
A _{7L}	13	36	A _{6R}
A _{8L}	14	35	A _{7R}
A _{9L}	15	34	A _{8R}
I/O _{0L}	16	33	A _{9R}
I/O _{1L}	17	32	I/O _{7R}
I/O _{2L}	18	31	I/O _{6R}
I/O _{3L}	19	30	I/O _{5R}
I/O _{4L}	20	29	I/O _{4R}
I/O _{5L}	21	28	I/O _{3R}
I/O _{6L}	22	27	I/O _{2R}
I/O _{7L}	23	26	I/O _{1R}
GND	24	25	I/O _{0R}

2720 drw 02



NOTES:

1. All Vcc pins must be connected to the power supply.
2. All GND pins must be connected to the ground supply.
3. P48-1 package body is approximately .55 in x 2.43 in x .18 in.
4. C48-2 package body is approximately .62 in x 2.43 in x .15 in.
5. J52-1 package body is approximately .75 in x .75 in x .17 in.
6. L48-1 package body is approximately .57 in x .57 in x .68 in.
7. F48-1 package body is approximately .75 in x .75 in x .11 in.
8. This package code is used to reference the package diagram.
9. This text does not indicate orientation of actual part-marking.

Absolute Maximum Ratings⁽¹⁾

Symbol	Rating	Commercial & Industrial	Military	Unit
VTERM ⁽²⁾	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
TBIAS	Temperature Under Bias	-55 to +125	-65 to +135	°C
TSTG	Storage Temperature	-65 to +150	-65 to +150	°C
PT ⁽³⁾	Power Dissipation	1.5	1.5	W
IOUT	DC Output Current	50	50	mA

2720 tbl 01

NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- VTERM must not exceed Vcc + 10% for more than 25% of the cycle time or 10 ns maximum, and is limited to $\leq 20\text{mA}$ for the period of $VTERM \geq Vcc + 10\%$.
- VTERM = 5.5V.

Recommended Operating Temperature and Supply Voltage^(1,2)

Grade	Ambient Temperature	GND	Vcc
Military	-55°C to +125°C	0V	5.0V \pm 10%
Commercial	0°C to +70°C	0V	5.0V \pm 10%
Industrial	-40°C to +85°C	0V	5.0V \pm 10%

2720 tbl 03

NOTES:

- This is the parameter TA. This is the "instant on" case temperature.

Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.5	5.0	5.5	V
GND	Ground	0	0	0	V
V _{IH}	Input High Voltage	2.2	—	6.0 ⁽²⁾	V
V _{IL}	Input Low Voltage	-0.5 ⁽¹⁾	—	0.8	V

2720 tbl 04

NOTES:

- V_{IL} (min.) $\geq -1.5\text{V}$ for pulse width less than 10ns.
- VTERM must not exceed Vcc + 10%.

Capacitance⁽¹⁾ (TA = +25°C, f = 1.0MHz)

Symbol	Parameter	Conditions ⁽²⁾	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 3dV	11	pF
C _{OUT}	Output Capacitance	V _{OUT} = 3dV	11	pF

2720 tbl 02

NOTES:

- This parameter is determined by device characterization but is not production tested.
- 3dV references the interpolated capacitance when the input and output signals switch from 0V to 3V and from 3V to 0V.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range (Vcc = 5V \pm 10%)

Symbol	Parameter	Test Conditions	7134SA		7134LA		Unit
			Min.	Max.	Min.	Max.	
I _{IL}	Input Leakage Current ⁽¹⁾	Vcc = 5.5V, V _{IN} = 0V to Vcc	—	10	—	5	µA
I _{LO}	Output Leakage Current	CĒ - V _{IH} , V _{OUT} = 0V to Vcc	—	10	—	5	µA
V _{OL}	Output Low Voltage	I _{OL} = 6mA	—	0.4	—	0.4	V
		I _{OL} = 8mA	—	0.5	—	0.5	V
V _{OH}	Output High Voltage	I _{OH} = -4mA	2.4	—	2.4	—	V

2720 tbl 05

NOTES:

- At Vcc $\leq 2.0\text{V}$ input leakages are undefined.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range^(1,2) (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Condition	Version	7134X20 Com'l Only		7134X25 Com'l, Ind & Military		7134X35 Com'l, Ind & Military		Unit	
				Typ.	Max.	Typ.	Max.	Typ.	Max.		
I _{CC}	Dynamic Operating Current (Both Ports Active)	$\bar{CE} = V_{IL}$ Outputs Disabled $f = f_{MAX}^{(3)}$	COM'L	SA LA	170 170	280 240	160 160	280 220	150 150	260 210	mA
			MIL & IND	SA LA	— —	— —	160 160	310 260	150 150	300 250	
I _{SB1}	Standby Current (Both Ports - TTL Level Inputs)	\bar{CE}_L and $\bar{CE}_R = V_{IH}$ $f = f_{MAX}^{(3)}$	COM'L	SA LA	25 25	100 80	25 25	80 50	25 25	75 45	mA
			MIL & IND	SA LA	— —	— —	25 25	100 80	25 25	75 55	
I _{SB2}	Standby Current (One Port - TTL Level Inputs)	$\bar{CE}_A^* = V_{IL}$ and $\bar{CE}_B^* = V_{IH}$ Active Port Outputs Disabled, $f=f_{MAX}^{(3)}$	COM'L	SA LA	105 105	180 150	95 95	180 140	85 85	170 130	mA
			MIL & IND	SA LA	— —	— —	95 95	210 170	85 85	200 160	
I _{SB3}	Full Standby Current (Both Ports - CMOS Level Inputs)	Both Ports \bar{CE}_L and $\bar{CE}_R \geq V_{CC} - 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$, $f = 0^{(3)}$	COM'L	SA LA	1.0 0.2	15 4.5	1.0 0.2	15 4.0	1.0 0.2	15 4.0	mA
			MIL & IND	SA LA	— —	— —	1.0 0.2	30 10	1.0 0.2	30 10	
I _{SB4}	Full Standby Current (One Port - CMOS Level Inputs)	One Port \bar{CE}_A^* or $\bar{CE}_B^* \geq V_{CC} - 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$ Active Port Outputs Disabled, $f = f_{MAX}^{(3)}$	COM'L	SA LA	105 105	170 130	95 95	170 120	85 85	160 110	mA
			MIL & IND	SA LA	— —	— —	95 95	210 150	85 85	190 130	

2720tbl06a

Symbol	Parameter	Test Condition	Version	7134X45 Com'l & Military		7134X55 Com'l, Ind & Military		7134X70 Com'l & Military		Unit	
				Typ.	Max.	Typ.	Max.	Typ.	Max.		
I _{CC}	Dynamic Operating Current (Both Ports Active)	$\bar{CE} = V_{IL}$ Outputs Disabled $f = f_{MAX}^{(3)}$	COM'L	SA LA	140 140	240 200	140 140	240 200	140 140	240 200	mA
			MIL & IND	SA LA	140 140	280 240	140 140	270 220	140 140	270 220	
I _{SB1}	Standby Current (Both Ports - TTL Level Inputs)	\bar{CE}_L and $\bar{CE}_R = V_{IH}$ $f = f_{MAX}^{(3)}$	COM'L	SA LA	25 25	70 40	25 25	70 40	25 25	70 40	mA
			MIL & IND	SA LA	25 25	70 50	25 25	70 50	25 25	70 50	
I _{SB2}	Standby Current (One Port - TTL Level Inputs)	$\bar{CE}_A^* = V_{IL}$ and $\bar{CE}_B^* = V_{IH}$ Active Port Outputs Disabled, $f=f_{MAX}^{(3)}$	COM'L	SA LA	75 75	160 130	75 75	160 130	75 75	160 130	mA
			MIL & IND	SA LA	75 75	190 150	75 75	180 150	75 75	180 150	
I _{SB3}	Full Standby Current (Both Ports - CMOS Level Inputs)	Both Ports \bar{CE}_L and $\bar{CE}_R \geq V_{CC} - 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$, $f = 0^{(3)}$	COM'L	SA LA	1.0 0.2	15 4.0	1.0 0.2	15 4.0	1.0 0.2	15 4.0	mA
			MIL & IND	SA LA	1.0 0.2	30 10	1.0 0.2	30 10	1.0 0.2	30 10	
I _{SB4}	Full Standby Current (One Port - CMOS Level Inputs)	One Port \bar{CE}_A^* or $\bar{CE}_B^* \geq V_{CC} - 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$ Active Port Outputs Disabled, $f = f_{MAX}^{(3)}$	COM'L	SA LA	75 75	150 100	75 75	150 100	75 75	150 100	mA
			MIL & IND	SA LA	75 75	180 120	75 75	170 120	75 75	170 120	

2720tbl06b

NOTES:

- 'X' in part number indicates power rating (SA or LA).
- V_{CC} = 5V, T_A = +25°C for typical, and parameters are not production tested.
- f_{MAX} = 1/t_{RC} = All inputs cycling at f = 1/t_{RC} (except Output Enable). f = 0 means no address or control lines change. Applies only to inputs at CMOS level standby I_{SB3}.

Data Retention Characteristics Over All Temperature Ranges
(LA Version Only) $V_{LC} = 0.2V$, $V_{HC} = V_{CC} - 0.2V$

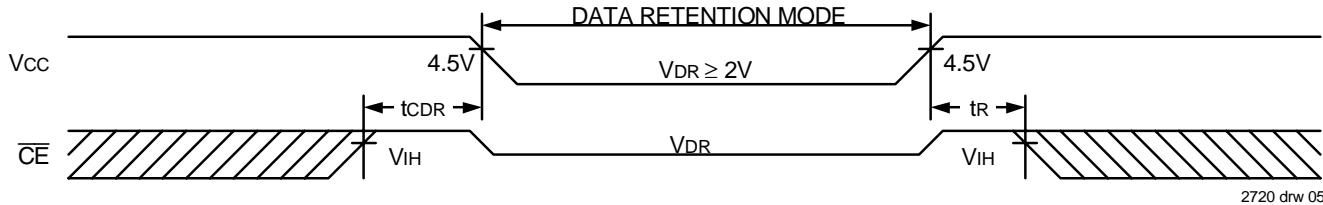
Symbol	Parameter	Test Condition	Min.	Typ. ⁽¹⁾	Max.	Unit
V_{DR}	V _{CC} for Data Retention	$V_{CC} = 2V$ $\overline{CE} \geq V_{HC}$ $V_{IN} \geq V_{HC}$ or $\leq V_{LC}$	2.0	—	—	V
I_{CDR}	Data Retention Current	MIL. & IND. COM'L.	—	100	4000	μA
$t_{CDR}^{(3)}$	Chip Deselect to Data Retention Time		—	100	1500	
$t_R^{(3)}$	Operation Recovery Time	0 $t_{RC}^{(2)}$	—	—	—	ns
			—	—	—	ns

2720 tbl 07

NOTES:

1. $V_{CC} = 2V$, $T_A = +25^\circ C$, and are not production tested.
2. t_{RC} = Read Cycle Time.
3. This parameter is guaranteed by device characterization, but not production tested.

Data Retention Waveform



AC Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	Figures 1 and 2

2720tbl 08

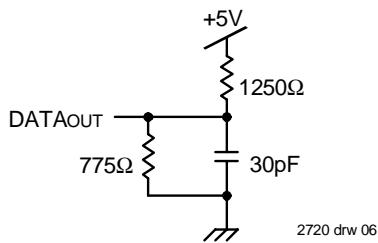


Figure 1. AC Output Test Load

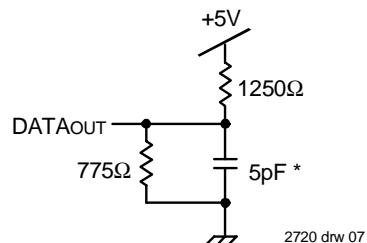


Figure 2. Output Test Load

(for t_{LZ} , t_{HZ} , t_{WZ} , t_{OW})

*Including scope and jig

AC Electrical Characteristics Over the
Operating Temperature and Supply Voltage⁽³⁾

Symbol	Parameter	7134X20 Com'l Only		7134X25 Com'l, Ind & Military		7134X35 Com'l, Ind & Military		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t _{RC}	Read Cycle Time	20	—	25	—	35	—	ns
t _{AA}	Address Access Time	—	20	—	25	—	35	ns
t _{ACE}	Chip Enable Access Time	—	20	—	25	—	35	ns
t _{AOE}	Output Enable Access Time	—	15	—	15	—	20	ns
t _{OH}	Output Hold from Address Change	0	—	0	—	0	—	ns
t _{LZ}	Output Low-Z Time ^(1,2)	0	—	0	—	0	—	ns
t _{HZ}	Output High-Z Time ^(1,2)	—	15	—	15	—	20	ns
t _{PU}	Chip Enable to Power Up Time ⁽²⁾	0	—	0	—	0	—	ns
t _{PD}	Chip Disable to Power Down Time ⁽²⁾	—	20	—	25	—	35	ns

2720 tbl 09a

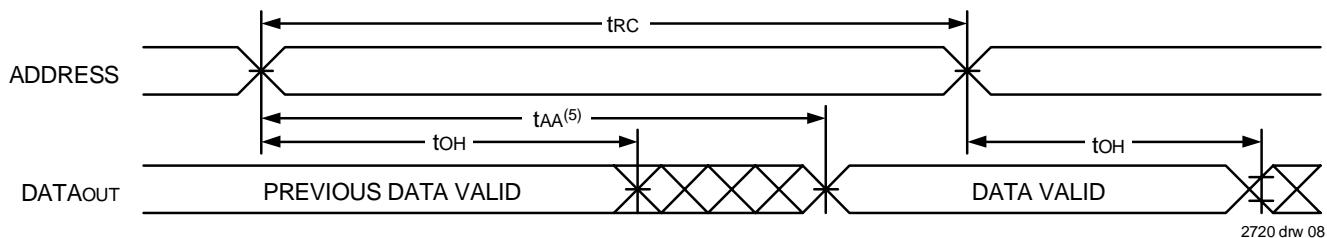
Symbol	Parameter	7134X45 Com'l & Military		7134X55 Com'l, Ind & Military		7134X70 Com'l & Military		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t _{RC}	Read Cycle Time	45	—	55	—	70	—	ns
t _{AA}	Address Access Time	—	45	—	55	—	70	ns
t _{ACE}	Chip Enable Access Time	—	45	—	55	—	70	ns
t _{AOE}	Output Enable Access Time	—	25	—	30	—	40	ns
t _{OH}	Output Hold from Address Change	0	—	0	—	0	—	ns
t _{LZ}	Output Low-Z Time ^(1,2)	5	—	5	—	5	—	ns
t _{HZ}	Output High-Z Time ^(1,2)	—	20	—	25	—	30	ns
t _{PU}	Chip Enable to Power Up Time ⁽²⁾	0	—	0	—	0	—	ns
t _{PD}	Chip Disable to Power Down Time ⁽²⁾	—	45	—	50	—	50	ns

2720 tbl 09b

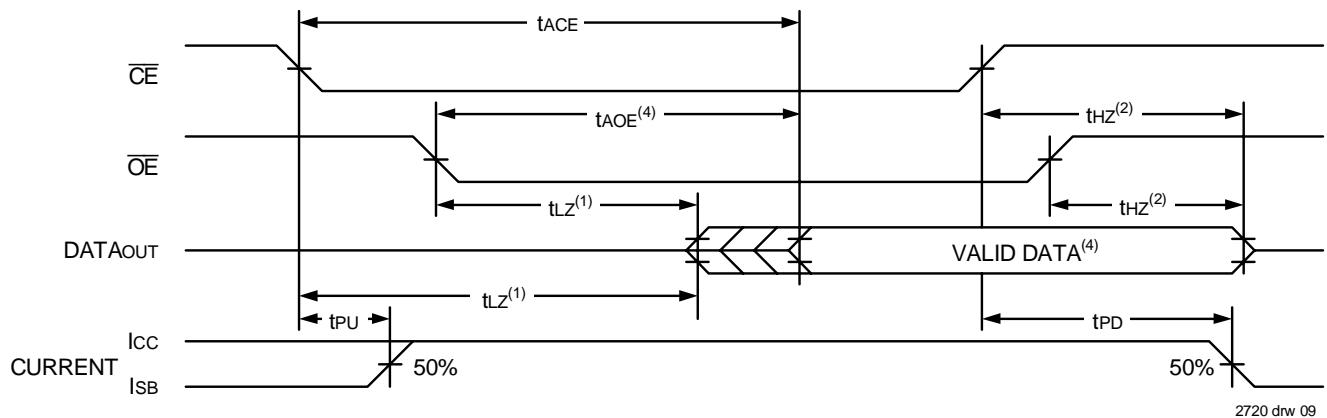
NOTES:

1. Transition is measured 0mV from Low or High-impedance voltage with the Output Test Load (Figure 2).
2. This parameter is guaranteed by device characterization, but is not production tested.
3. 'X' in part number indicates power rating (SA or LA).

Timing Waveform of Read Cycle No. 1, Either Side^(1,2,4)



Timing Waveform of Read Cycle No. 2, Either Side^(1,3)



NOTES:

1. Timing depends on which signal is asserted last, \overline{OE} or \overline{CE} .
2. Timing depends on which signal is de-asserted first, OE or CE .
3. $R/W = V_{IH}$.
4. Start of valid data depends on which timing becomes effective, tAOE, tACE or tAA.
5. tAA for RAM Address Access and tsAA for Semaphore Address Access.

AC Electrical Characteristics Over the
Operating Temperature and Supply Voltage⁽⁵⁾

Symbol	Parameter	7134X20 Com'l Only		7134X25 Com'l, Ind & Military		7134X35 Com'l, Ind & Military		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
WRITE CYCLE								
t _{WC}	Write Cycle Time	20	—	25	—	35	—	ns
t _{EW}	Chip Enable to End-of-Write	15	—	20	—	30	—	ns
t _{AW}	Address Valid to End-of-Write	15	—	20	—	30	—	ns
t _{AS}	Address Set-up Time	0	—	0	—	0	—	ns
t _{WP}	Write Pulse Width	15	—	20	—	25	—	ns
t _{WR}	Write Recovery Time	0	—	0	—	0	—	ns
t _{DW}	Data Valid to End-of-Write	15	—	15	—	20	—	ns
t _{HZ}	Output High-Z Time ^(1,2)	—	15	—	15	—	20	ns
t _{DH}	Data Hold Time ⁽³⁾	0	—	0	—	3	—	ns
t _{WZ}	Write Enable to Output in High-Z ^(1,2)	—	15	—	15	—	20	ns
t _{OW}	Output Active from End-of-Write ^(1,2,3)	3	—	3	—	3	—	ns
t _{WDD}	Write Pulse to Data Delay ⁽⁴⁾	—	40	—	50	—	60	ns
t _{DD}	Write Data Valid to Read Data Delay ^(4,6)	—	30	—	30	—	35	ns

2720 tbl 10a

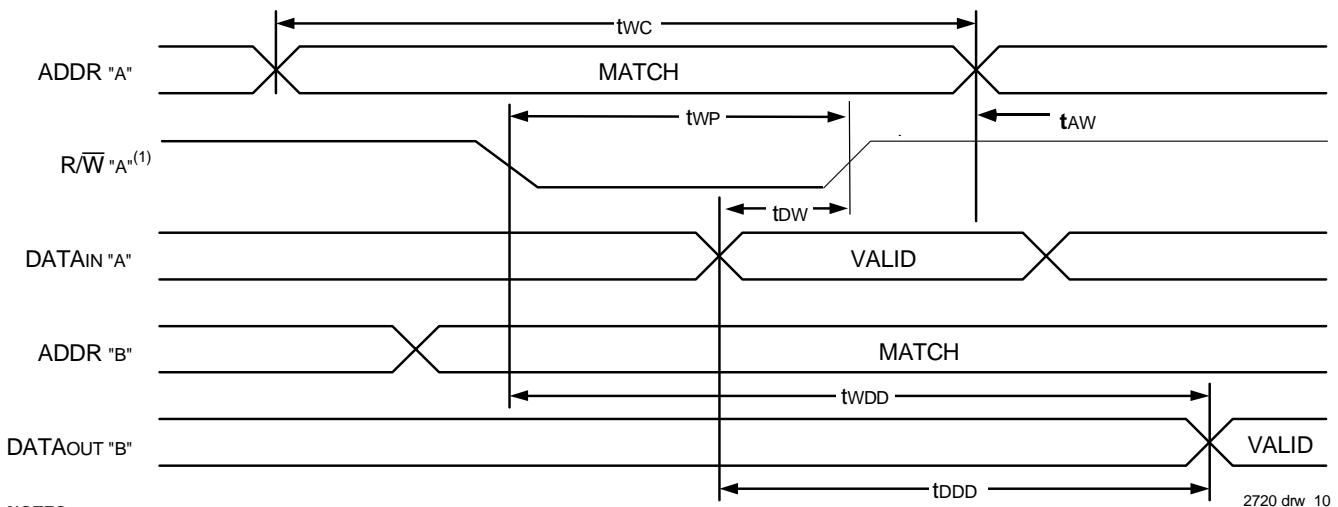
Symbol	Parameter	7134X45 Com'l & Military		7134X55 Com'l, Ind & Military		7134X70 Com'l & Military		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
WRITE CYCLE								
t _{WC}	Write Cycle Time	45	—	55	—	70	—	ns
t _{EW}	Chip Enable to End-of-Write	40	—	50	—	60	—	ns
t _{AW}	Address Valid to End-of-Write	40	—	50	—	60	—	ns
t _{AS}	Address Set-up Time	0	—	0	—	0	—	ns
t _{WP}	Write Pulse Width	40	—	50	—	60	—	ns
t _{WR}	Write Recovery Time	0	—	0	—	0	—	ns
t _{DW}	Data Valid to End-of-Write	20	—	25	—	30	—	ns
t _{HZ}	Output High-Z Time ^(1,2)	—	20	—	25	—	30	ns
t _{DH}	Data Hold Time ⁽³⁾	3	—	3	—	3	—	ns
t _{WZ}	Write Enable to Output in High-Z ^(1,2)	—	20	—	25	—	30	ns
t _{OW}	Output Active from End-of-Write ^(1,2,3)	3	—	3	—	3	—	ns
t _{WDD}	Write Pulse to Data Delay ⁽⁴⁾	—	70	—	80	—	90	ns
t _{DD}	Write Data Valid to Read Data Delay ^(4,6)	—	45	—	55	—	70	ns

NOTES:

1. Transition is measured 0mV from Low or High-impedance voltage with Output Test Load (Figure 2).
2. This parameter is guaranteed by device characterization, but is not production tested.
3. The specification for t_{DH} must be met by the device supplying write data to the RAM under all operating conditions. Although t_{DH} and tow values will vary over voltage and temperature, the actual t_{DH} will always be smaller than the actual tow.
4. Port-to-port delay through RAM cells from writing port to reading port, refer to "Timing Waveform of Write with Port-to-Port Read".
5. 'X' in part number indicates power rating (SA or LA).
6. t_{DD} = 35ns for military temperature range.

2720 tbl 10b

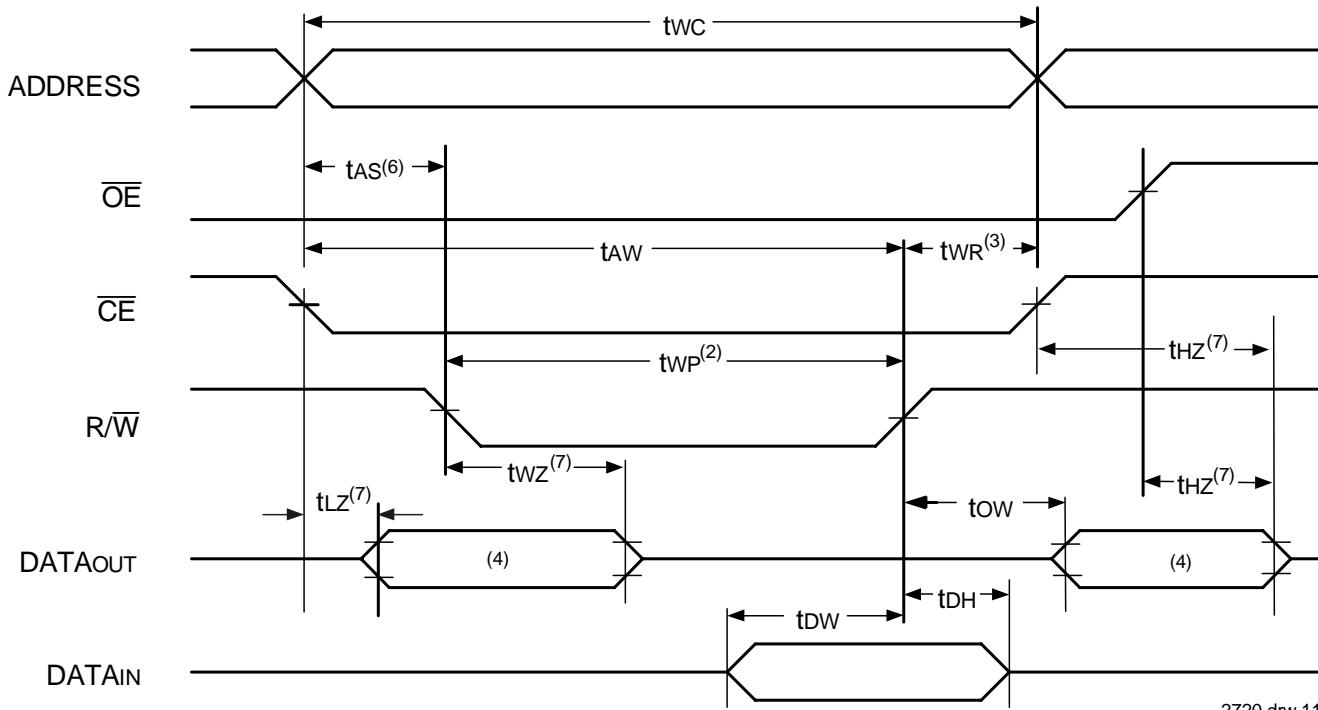
Timing Waveform of Write with Port-to-Port Read^(1,2,3)



NOTES:

1. Write cycle parameters should be adhered to, in order to ensure proper writing.
2. $\overline{CE} = \overline{CE}_R = V_{IL}$, $\overline{OE}^B = V_{IL}$.
3. Port "A" may be either left or right port. Port "B" is the opposite from port "A".

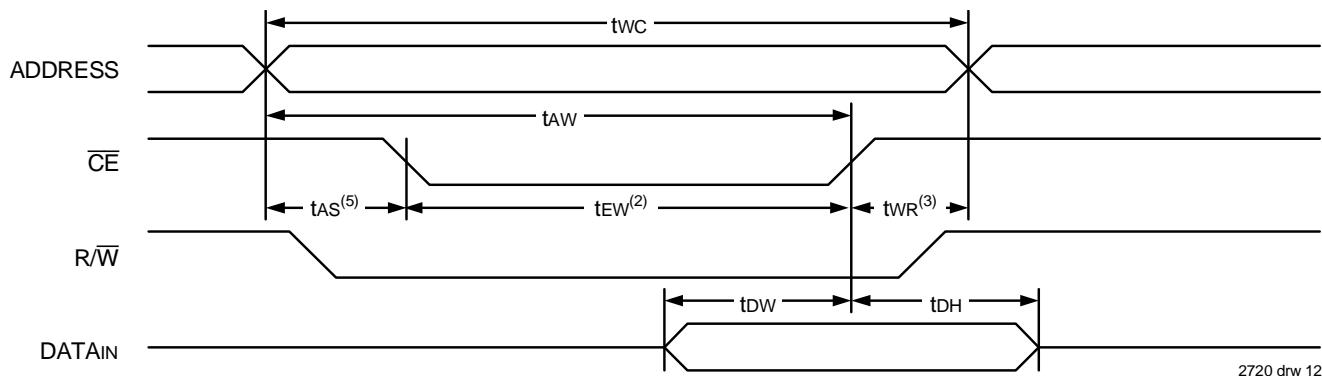
Timing Waveform of Write Cycle No. 1, R/W Controlled Timing^(1,5,8)



NOTES:

1. R/W or \overline{CE} must be HIGH during all address transitions.
2. A write occurs during the overlap (tew or twp) of a $\overline{CE} = V_{IL}$ and $R/W = V_{IL}$.
3. twr is measured from the earlier of \overline{CE} or R/W going to V_{IH} to the end-of-write cycle.
4. During this period, the I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CE} = V_{IL}$ transition occurs simultaneously with or after the $R/W = V_{IL}$ transition, the outputs remain in the High-impedance state.
6. Timing depends on which enable signal (\overline{CE} or R/W) is asserted last.
7. This parameter is guaranteed by device characterization, but is not production tested. Transition is measured 0mV from steady state with the Output Test Load (Figure 2).
8. If $\overline{OE} = V_{IL}$ during a R/W controlled write cycle, the write pulse width must be the larger of twp or (twz + tow) to allow the I/O drivers to turn off data to be placed on the bus for the required tow. If $\overline{OE} = V_{IH}$ during an R/W controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified twp.

Timing Waveform of Write Cycle No. 2, **CE** Controlled Timing^(1,4)



NOTES:

1. \overline{RW} or \overline{CE} must be HIGH during all address transitions.
2. A write occurs during the overlap (t_{EW} or t_{DW}) of a $\overline{CE} = V_{IL}$ and $\overline{RW} = V_{IL}$.
3. t_{WR} is measured from the earlier of \overline{CE} or \overline{RW} going HIGH to the end-of-write cycle.
4. If the \overline{CE} LOW transition occurs simultaneously with or after the \overline{RW} LOW transition, the outputs remain in the High-impedance state.
5. Timing depends on which enable signal (\overline{CE} or \overline{RW}) is asserted last.

Functional Description

The IDT7134 provides two ports with separate control, address, and I/O pins that permit independent access for reads or writes to any location in memory. These devices have an automatic power down feature controlled by \overline{CE} . The \overline{CE} controls on-chip power down circuitry that permits the respective port to go into standby mode when not selected (\overline{CE} HIGH). When a port is enabled, access to the entire memory array is permitted. Each port has its own Output Enable control (\overline{OE}). In the read mode, the port's \overline{OE} turns on the output drivers when set LOW. Non-contention READ/WRITE conditions are illustrated in Truth Table I.

Truth Table I – Read/Write Control

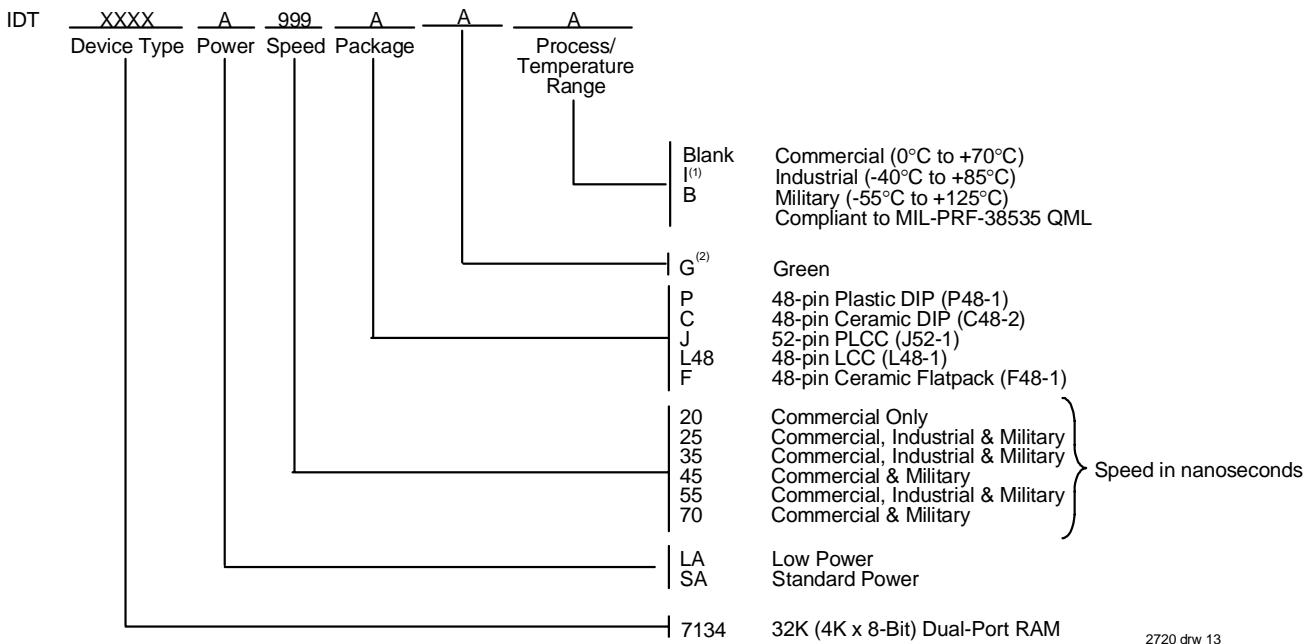
Left or Right Port ⁽¹⁾				
\overline{RW}	\overline{CE}	\overline{OE}	Do-7	Function
X	H	X	Z	Port Deselected and in Power-Down Mode, lsB2 or lsB4
X	H	X	Z	$\overline{CE}_R = \overline{CE}_L = H$, Power Down Mode lsB1 or lsB3
L	L	X	DATAIN	Data on port written into memory
H	L	L	DATAOUT	Data in memory output on port
X	X	H	Z	High impedance outputs

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NOTE:

1. $A_{0L} - A_{11L} \neq A_{0R} - A_{11R}$
 $"H" = V_{IH}$, $"L" = V_{IL}$, $"X" = \text{Don't Care}$, and $"Z" = \text{High Impedance}$

Ordering Information



NOTES:

1. Contact your local sales office for industrial temp. range for other speeds, packages and powers.
2. Green parts available. For specific speeds, packages and powers contact your local sales office.

Datasheet Document History

03/25/99:		Initiated datasheet document history Converted to new format Cosmetic and typographical corrections
060/9/99:	Pages 2	Added additional notes to pin configurations Changed drawing format
10/01/99:		Added Industrial Temperature Ranges and removed corresponding notes
11/10/99:		Replaced IDT logo
12/22/99:	Page 1	Made corrections to drawing
03/03/00:		Corrected block diagram and pin configurations Changed ±500mV to 0mV
01/12/00:	Pages 1 2	Moved "Description" to page 2 and adjusted page layout
	Page 1	Added "LA only" to paragraph
	Page 2	Fixed P48-1 package description
	Page 3	Increased storage temperature parameters Clarified TA parameter
	Page 4	DC Electrical parameters—changed wording from "open" to "disabled"
	Page 10	Fixed Truth Table specification in "Functional Description" paragraph
01/17/06:	Page 1	Added green availability to features
	Page 11	Added green indicator to ordering information
	Page 1 & 11	Replaced old IDT™ with new IDT™ logo



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